

1 Vivado 2018.2 SDK ModelSim
 2 xc7z020clg400-2 FPGA
 3
 (1) IMX2221 Bayer RGB
 (2) DMA DDR3 hdmi hdmi DDR3 PS
 (3) DMA DDR3 hdmi hdmi
 HDMI
 (4) HDMI 60HZ 1080P SD

1 Vivado 2018.2 Modelsim Matlab Wireshark
 2 xc7a75tfgg484-2 FPGA
 3
 (1) Matlab UDP Matlab mat
 (2) RJ45 PHY FPGA PHY RGMII
 (3) FPGA IDDR_CTRL PHY PHY PHY
 125MHz 4bit 125x4x2=1000Mbps DDR_CTRL MIG IP
 HDMI HDMI ODDR_CTRL
 UDP
 (4) HDMI 1024x768@ 60Hz Wireshark
 UDP CRC

1 Vivado 2018.2 VS2015
 2 xc7a75tfgg484-2 FPGA
 3
 (1) Riffa PCIe PC Riffa API Riffa TLP
 VS2015 MFC Riffa API Riffa
 PC Riffa
 API
 (2) Riffa 2 Riffa
 DDR_CTRL MIG IP DDR3 HDMI
 HDMI
 (3) HDMI PC 1080P 800MBps

- 1. Verilog HDL RTL Testbench C/Matlab
 2. FPGA Modelsim ILA ChipScope 3.
 Xilinx ISE Vivado Xilinx Spartan6 Artix7
 4. Linux Spyglass/VCS/Verdi Makefile 5.

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- CET-6

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